REMARKS

Favorable reconsideration of the present application as currently constituted is respectfully requested.

Current Status of the Claims

Claims 1-49 are pending, of which claims 1, 22 and 35 are in independent form. Claims 1, 6-14, 22 and 35 are currently amended. Claims 2-5, 15-21, 23-34 and 36-49 are in original form.

Support for the claim amendments may be found at, inter alia, paragraphs [0021], [0034], [0035] and [0036]-[0040] of the original Specification.

Regarding Amendments to the Specification

Minor typographical errors have been rectified by way of suitable amendments to the Specification as set forth hereinabove. No new matter is introduced hereby.

Regarding the Claim Rejections - 35 U.S.C. § 102

In the pending Office Action, claims 1-49 stand rejected under 35 U.S.C. §102(e) as being anticipated by U.S. Patent Application Publication No. US 2001/0052062 to Lipovski (hereinafter the *Lipovski* reference). The following comments are provided with respect to these §102 rejections:

As to claims 1 (method), 22 (system) and 35 (machine-readable medium), Lipovski teaches a memory characterization method comprising the steps generating a plurality of tiles forming a memory instance, said plurality of tiles including at least one of the sub-plurality of row decoder tiles, a sub plurality of input/output (I/O) block tiles, a sub plurality of bitcell array tiles and at least one control block tile (see fig 2 and fig 5 element 13 col 8 lines 35-53); providing input and output for each tile to with respect to a plurality of global signals spanning said memory instance in at least one of the horizontal and a vertical direction (see fig 2 and fig 5 and fig 6); obtaining a parametric dataset for each of said plurality of tiles (see col 9 lines 3-45); and creating a hierarchically-stitched parametric netlist for said memory instance by coupling said parametric datasets using said input and output pins for said plurality of tiles with respect to said global signals (see fig 2 and fig 5 and fig 6 col 9 lines 3-45).

As to claims 2 (method), and 49 (machine-readable medium), Lipovski teaches wherein said tiles are generated based on a minimum area required to encompass an optimal number of memory straps points associated with at least a portion of said global signals (see fig 5-6 col 9 and background).

As to claims 3, 6 (method), and 36 (machine-readable medium), Lipovski teaches wherein said memory instance comprises a post-layout schema, and further wherein said step of obtaining a parametric dataset for each of said plurality of tiles comprises extracting an RC netlist from a select portion of: said post-layout schema corresponding to a particular tile (see fig 7 col 10 lines 20-48).

As to claims 4, 5 (method), 23 (system) and 37 (machine-readable medium), Lipovski teaches wherein said memory instance comprises a pre layout schema, and further wherein said step of obtaining a parametric dataset for each of said plurality of tiles comprises estimating RC parametric data corresponding to a particular tile based on its wire-delay model circuit (see fig 5-6 background/summary).

As to claims 7-10 Lipovski teaches wherein said plurality of tiles are generated from a memory instance comprising a read-only memory (ROM), (RAM), (DRAM), and (EPROM) circuit (see fig 5-6 background/summary).

As to claims 11 (method), 24 (system) and 38 (machine-readable medium), Lipovski teaches wherein said plurality of tiles are generated from a memory instance comprising a flash memory circuit (see fig 5-6 background/summary).

As to claims 12 (method), 26 (system) and 40 (machine-readable medium), Lipovski teaches wherein said plurality of tiles are generated from a memory instance comprising a compilable memory circuit (see fig 5-6 background/summary).

As to claims 13 (method), 25 (system) and 39 (machine-readable medium), Lipovski teaches wherein said plurality of tiles are generated from a memory instance comprising an embedded memory circuit (see fig 5-6 background/summary).

As to claims 14 (method), 27 (system) and 41 (machine-readable medium), Lipovski teaches wherein said plurality of tiles are generated from a memory instance comprising a stand-

alone memory circuit (see fig 5-6 background/summary).

As to claims 15 (method), 28 (system) and 42 (machine-readable medium), Lipovski teaches wherein said global signals comprise a plurality of pre-decoder signals emanating from said at least one control block tile, said pre-decoder signals being operable to couple said sub-plurality of row decoder tiles in a head-to-tail fashion along said vertical direction (see fig 5-6 and col 9-10 background/summary).

As to claims 16 (method), 29 (system) and 43 (machine-readable medium), Lipovski teaches wherein each row decoder tile is coupled to a corresponding portion of said plurality of wordline signals, said corresponding portion being operable to couple a select row of said sub-plurality of bitcell array tiles in a head-to-tail fashion along said horizontal direction (see fig 5-6 and col 9-10 background/summary).

As to claims 17 (method), 30 (system) and 44 (machine-readable medium), Lipovski teaches wherein each row decoder tile is coupled to a corresponding portion of said plurality of wordline signals, said corresponding portion being operable to couple a select row of said sub-plurality of bitcell array tiles in a head-to-tail fashion along said horizontal direction (see fig 5-6 and col 9-10 background/summary).

As to claims 18 (method), 31 (system) and 45 (machine-readable medium), Lipovski teaches wherein said global signals comprise a plurality of control signals emanating from said at least one control block tile, said control signals being operable to couple said sub-plurality of I/O block tiles in a head-to-

tail fashion along said horizontal direction (see fig 5-6 and col 9-10 background/summary).

As to claims 19 (method), 32 (system) and 46 (machine-readable medium), Lipovski teaches wherein said global signals comprise a plurality of bitline signals emanating from said sub plurality of I/O block tiles (see fig 5-6).

As to claims 20 (method), 33 (system) and 47 (machine-readable medium), Lipovski teaches wherein each I/O block tile is coupled to a corresponding portion of said plurality of bitline signals, said corresponding portion being operable to couple a select column of said sub-plurality of bitcell array tiles in a head-to-tail fashion along said vertical direction (see fig 5-6 and col 9-10 background/summary).

As to claims 21 (method), 34 (system) and 48 (machine-readable medium), Lipovski teaches wherein said global signals comprise a plurality of power lines coupling said sub-plurality of I/O block tiles with said sub-plurality of bitcell array tiles in said vertical direction (see fig 5-6 and col 9-10 background/summary).

Applicant respectfully submits that the pending §102 rejections have been overcome or otherwise rendered moot by the present claim amendments. As currently constituted, the present invention is directed to a memory characterization method and system as well as associated computer-accessible medium, wherein a plurality of tiles operable to model a memory instance are

generated. Each tile is provided with input and output pins with respect to a plurality of global signals that span the memory instance in a horizontal direction, a vertical direction, or both. A hierarchically-stitched parametric netlist that simulates the memory instance is created by coupling individual parametric datasets obtained for each tile, which are coupled using the input and output pins with respect to the global signals.

It is respectfully contended herein that the *Lipovski* reference does not anticipate or even remotely allude to the present invention as currently claimed. The *Lipovski* reference discloses a dynamic storage device that incorporates logic circuitry within the refresh circuitry of a dynamic RAM, thereby allowing logical removal, or bypassing, of faulty cells. See *Lipovski* at Paragraph [0013], Summary of the Invention. In other words, the dynamic storage device of the *Lipovski* reference provides a way to incorporate redundancy within the context of a DRAM integrated with processor circuitry (i.e., processor-in-memory or logic-in-memory devices) that gives rise to improved fabrication yields. See *Lipovski* at Paragraph [0006], Background of the Invention; see also *Lipovski* at Paragraph [0013], Summary of the Invention.

Applicant respectfully submits that Figures 2, 5 and 6 and related description in the *Lipovski* reference do not teach or suggest the claimed memory characterization system and method where a plurality of tiles that model a memory instance are generated for creation of a hierarchically-stitched netlist that simulates the memory instance. Figure 2 of the *Lipovski* reference is merely a schematic representation of a prior art DRAM. Figure 5 is a block diagram of a one-megabit DRAM employing logic in its refresh circuitry. Figure 6 is a block diagram of another DRAM that employs logic its refresh circuitry. The related description provided at column 9, lines 3-45 (Paragraphs 0065 - 0068) of the *Lipovski* reference discloses a dynamic associative access memory operation. As provided in the Abstract of the *Lipovski* reference, the individual storage positions of a dynamic storage device (i.e., DRAM with logic in its refresh circuitry) are periodically read by a refresh amplifier, then a logical operation is performed on the refresh data before application to the write amplifier, allowing implementation of associative data base searching by cyclically executing data compare and other logical operations within the refresh circuitry. There is absolutely no anticipation or suggestion therein relative to the claimed memory

characterization scheme using a hierarchically-stitched netlist that simulates the memory instance, which netlist is created based on parametric datasets of individual tiles representing the memory instance.

Based on the foregoing discussion, Applicant respectfully submits that the independent claims 1, 22 and 35 are allowable over the applied art. Dependent claims 2-21, 23-34 and 36-49 respectively depend from these three base claims and introduce additional limitation therein. Accordingly, the dependent claims of the present patent application are also allowable.

Regarding the Art Cited but not Relied Upon

Applicant appreciates the inclusion of the art cited but not relied upon in the pending Office Action. Upon review thereof, it is believed that the currently claimed invention is patentable over the entire art made of record.

SUMMARY AND CONCLUSION

In view of the foregoing, the Examiner is respectfully requested to reconsider and withdraw the outstanding objections and rejections and allow claims 1-49 presented for reconsideration herein. Accordingly, a favorable action in the form of an early notice of allowance is respectfully requested.

Respectfully submitted,

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